

CS 315-01 RISC-V Machine Code

Bitwise operators in RISC-V

and / andi

or / ori

xor / xori

sll / slli

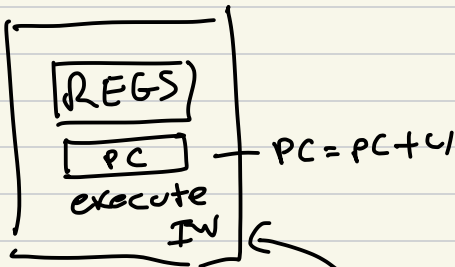
srl / srli

sra / srai

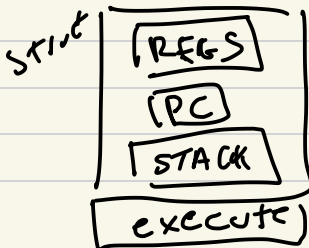
and t_0, t_1, t_2

$\# t_0 = t_1 \& t_2$

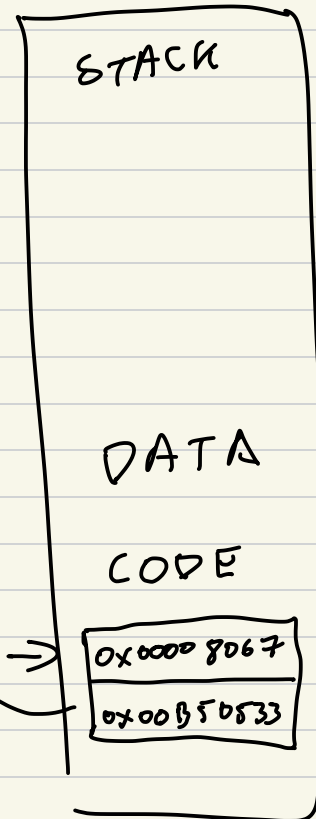
RISC-V Processor



RISC-V Emulator



Memory



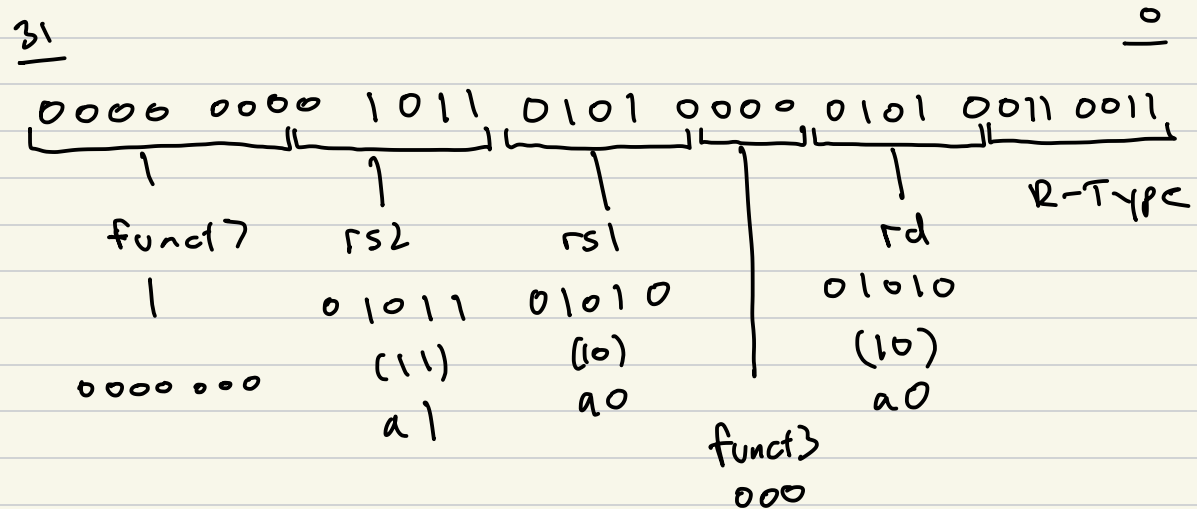
Processor State

Registers (32) 64 bit values
uint64_t

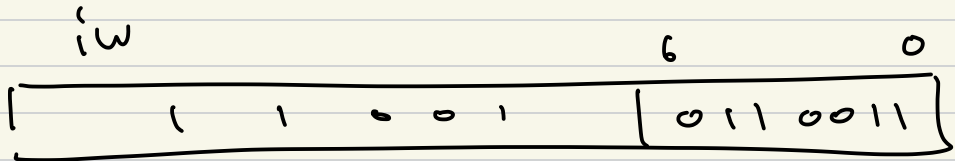
PC uint64_t
Program Counter

Memory $\left\{ \begin{array}{l} \text{STACK} \\ \text{CODE} \\ \text{DATA} \end{array} \right.$

add $\frac{a0}{rd}, \frac{a0}{rs1}, \frac{a1}{rs2}$
iw = 0x00B50533



Masking



Mask $\&$

0b 00 0 1 1 1 1 1 1

0 0 0 0 1 1 0 0 1 1

rv-state

SP

Stack[8191]

regs[32]

pc
stack

stack[0]

