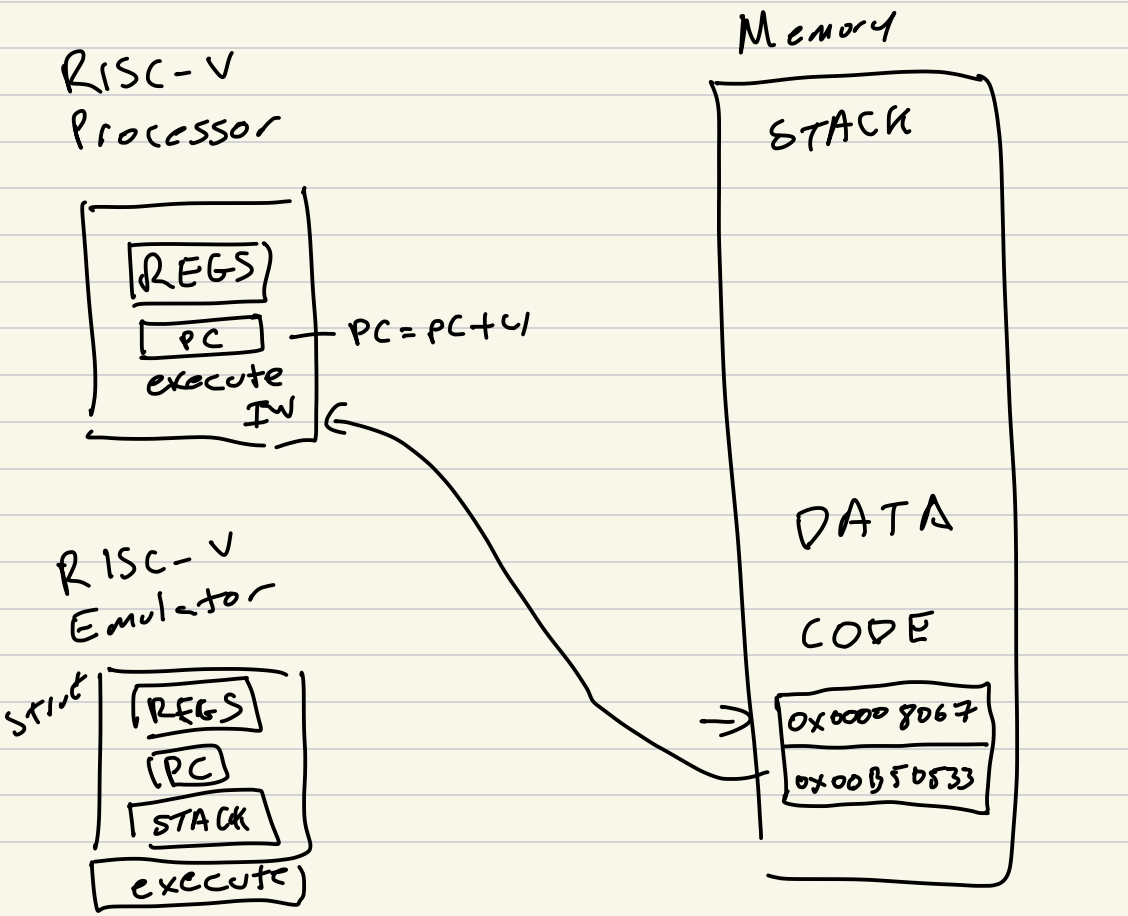
CS 315-01 RISC-V Machine Code

Bitwise operators in RISC-V

```
and / and:
or  / or:
xor / xor:
sll / sll:
srl / srl:
sra / sra:
```

```
and t0, t1, t2
# t0 = t1 & t2
```



Processor State

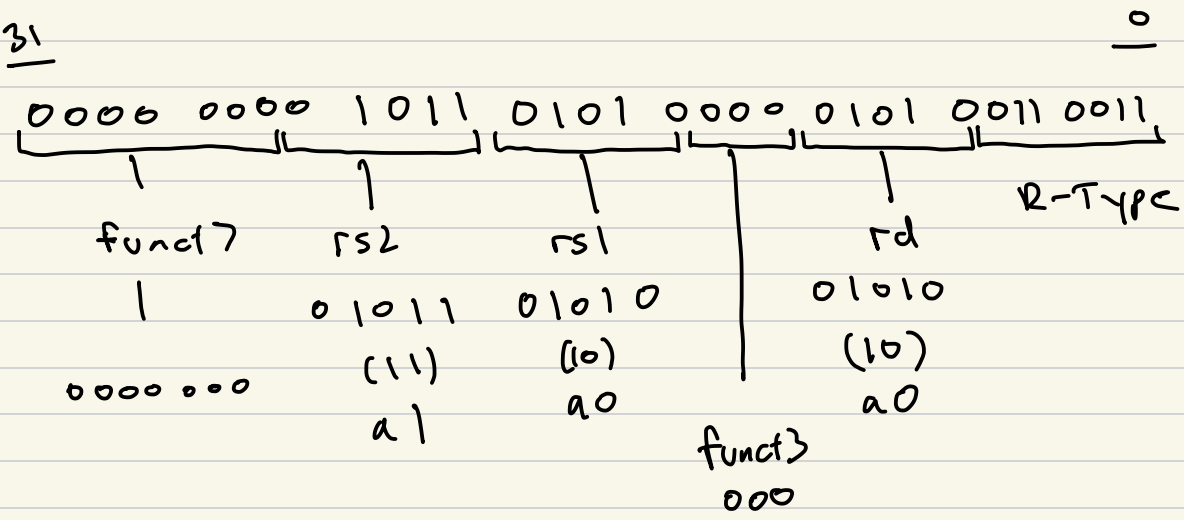
Registers (32) 64 bit values
uint64_t

PC uint64_t
Program Counter

Memory — STACK
CODE
DATA

add a0, a0, a1
rd rs1 rs2

iw = 0x00B50533



Masking